MAXLINEAR

MXL101SF
DVB-T INTEGRATED RECEIVER

General Description

The MxL101SF is a single-chip integrated tuner and demodulator receiver IC. It meets the specifications of digital DVB-T TV standards (NorDig Unified 2.0, MBRAI and DTG). The MxL101SF has a built-in I2C interface. It enables the implementation of DVB-T receiver functionality in a very small footprint with low BOM cost and low power consumption.

The MxL101SF can be configured into either Tuner-Demod or Tuner mode. In Tuner-Demod mode, the on-chip demodulator is activated to output MPEG-2 TS data. In tuner mode, the tuner outputs an analog IF signal. Gain control, LO generation, and channel selectivity functions are completely integrated on the chip, which simplifies board-level design. The IC requires 3.3V and 1.8V supplies.

The MxL101SF is available in a 7 x 7 mm² 48-pin QFN package.

Applications

- High-performance DVB-T television receivers
- Set-Top Boxes
- Flat-screen TVs with low power and small form-factor requirements
- Portable applications such as laptops, portable DVD players
- Handheld applications such as cellular phones and PDAs

Features (Tuner-Demod Mode)

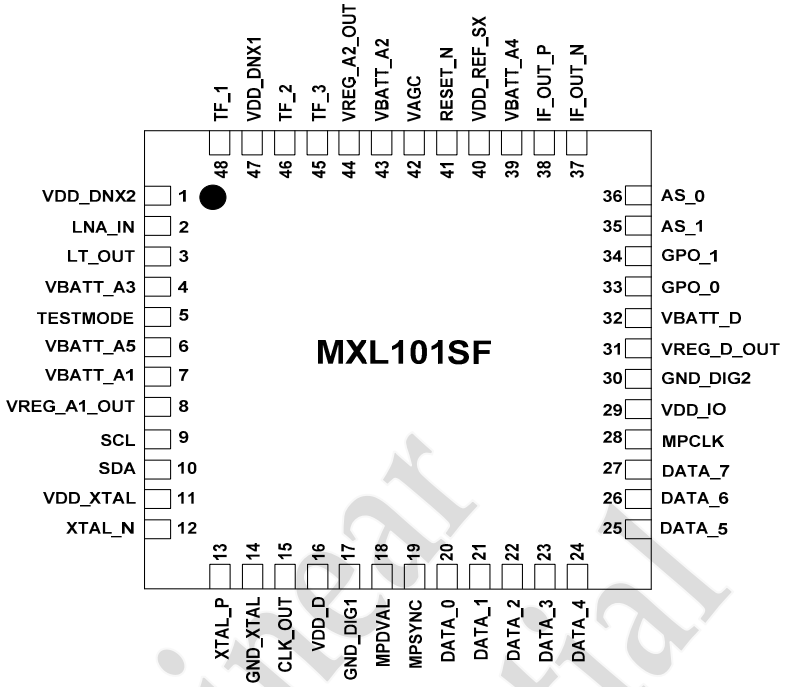
- Tuning range from 104 to 862 MHz
- NorDig 2.0 and MBRAI compliant
  - No external LNA required
- Single LNA input pin for all bands
- Integrated channel filtering requiring no external SAW filters
- Programmable channel bandwidths of 6, 7, or 8MHz
- Automatic channel mode detection and fast locking time
- Dual supply of 3.3V and 1.8V operation using on-chip regulators
  - It can also use an additional external 1.2V supply for low power option
- Low-power consumption of 475 mW typical in UHF band
- MPEG video Serial or parallel output
- On-chip RF loopthrough
- Two General Purpose output interface pins for controlling off-chip circuitry

Features (Tuner Mode)

(In addition to tuner-demod mode where applicable)

- Tuning range from 44 to 885 MHz
- Programmable IF frequency
- Programmable IF spectrum inversion
- Low power consumption of 384 mW typical in UHF

Pin Configuration



IC Block Diagram

The architecture of the DVB-T integrated receiver is illustrated in the functional block diagram of Figure 1. The device incorporates a fully-integrated tuner and demodulator. On-chip regulators regulate the battery voltage to the internal supplies of 1.6 and 1.2V. There are two modes of operation:

(1) Tuner-Demod mode: which activates the demodulator to provide demodulated DVB-T MPEG-2 TS serial or parallel data output.

(2) Tuner mode: In this mode the demodulator is deactivated. The tuner outputs an analog IF signal.

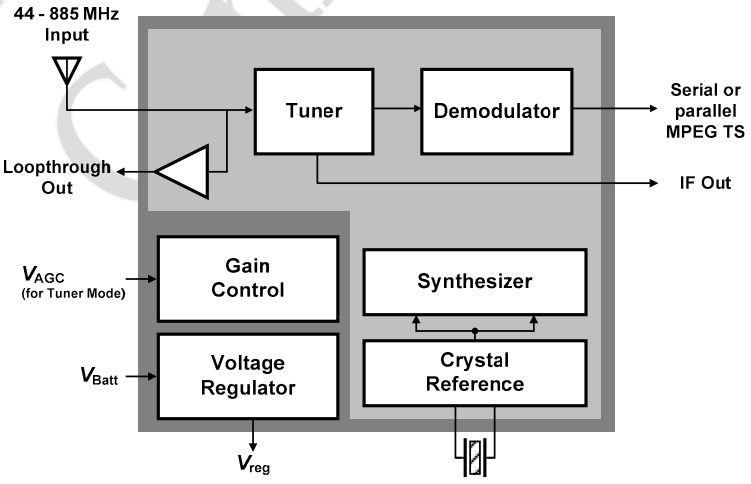


Figure 1: Simplified block diagram

Pin Description

Pin Names

Pin #	Pin Name		Pin #	Pin Name
1	VDD_DNX2		25	DATA_5
2	LNA_IN		26	DATA_6
3	LT_OUT		27	DATA_7
4	VBATT_A3		28	MPCLK
5	TESTMODE		29	VDD_IO
6	VBATT_A5		30	GND_DIG2
7	VBATT_A1		31	VREG_D_OUT
8	VREG_A1_OUT		32	VBATT_D
9	SCL		33	GPO_0
10	SDA		34	GPO_1
11	VDD_XTAL		35	AS_1
12	XTAL_N		36	AS_0
13	XTAL_P		37	IF_OUT_N
14	GND_XTAL		38	IF_OUT_P
15	CLK_OUT		39	VBATT_A4
16	VDD_D		40	VDD_REF_SX
17	GND_DIG1		41	RESET_N
18	MPDVAL		42	VAGC
19	MPSYNC		43	VBATT_A2
20	DATA_0		44	VREG_A2_OUT
21	DATA_1		45	TF_3
22	DATA_2		46	TF_2
23	DATA_3		47	VDD_DNX1
24	DATA_4		48	TF_1

RF Interface

Pin Name	Direction	Description
LNA_IN	Input	Single-ended RF input with input impedance of 75Ω. It can also be used as the on-chip loopthrough input

Loopthrough Interface

Pin Name	Direction	Description
LT_OUT	Output	On-chip Loopthrough output with open drain

I²C Interface

This chip is an I2C slave. I2C interface is used to configure and program the device.

Pin Name	Direction	Description
SCL	input	Clock
SDA	Bi-dir	Data

Supply and Ground

This device contains on-chip regulators that regulate the battery voltage to lower voltages for on-chip operation.

Pin Name	Direction	Description
VDD_DNX2, VDD_XTAL, VDD_D, VDD_REF_SX, VDD_DNX1	Input	Supply voltage for on-chip circuits
VBATT_A3, VBATT_A4, VBATT_A5	Input	Supply voltage input for on-chip blocks
VBATT_A1, VBATT_A2	Input	Supply voltage input for on-chip analog regulators
VREG_A1_OUT, VREG_A2_OUT	Output	On-chip analog regulators output
VBATT_D	Input	Supply voltage input for on-chip digital regulator
VREG_D_OUT	Output	On-chip digital regulator output. Internally connected to VDD_D
GND_DIG1, 2	Input	Ground for digital circuit blocks
VDD_IO	Input	Supply voltage input for I/O interface
GND_XTAL	Input	Ground for crystal supply

Analog and Digital I/O

Pin Name	Direction	Description
XTAL_P	Input	Crystal positive input. It can be used as an external system clock input pin if no crystal is used.
XTAL_N	Input	Crystal negative input
MPDVAL	Output	MPEG parallel and serial data valid. This pin has internal pull down.
MPSYNC	Output	MPEG parallel and serial frame synch. This pin has internal pull down.
DATA_0 - 7	Output	MPEG outputs. These pins have internal pull down. DATA_0 is used for serial mode. DATA_1-7 can be GPOs when not in use.
MPCLK	Output	MPEG parallel and serial clock output. This pin has internal pull down.
GPO_0 - 1	Output	General purpose outputs
AS_0 – 1	Input	I2C address select. These pins have internal pull down.
IF_OUT_P	Output	IF output
IF_OUT_N	Output	IF output
TESTMODE	Input	Reserved for internal use
VAGC	Input	For tuner mode only. Single automatic gain control. The partitioning is controlled on-chip.
TF_1-3	Bi-dir	Pins used for input broadband filtering
CLK_OUT	Output	Reuse of crystal clock to share with other devices
RESET_N	Input	If this pin is grounded, the device goes to sleep state. This pin has internal pull up.

Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units
VBATT_A1, A2, A3, A4, A5	0	3.6	V
VBATT_D	0	3.6	V
VDD_IO	0	3.6	V
VDD_D	0	1.5	V
VAGC	0	3.6	V
All other VDD_NAME	0	1.8	V
VREG_D_OUT	0	1.5	V
SDA, SCL	0	3.6	V
RF Input Power		10	dBm
Storage Temp	-65	150	°C
Junction Temp		150	°C
Soldering Temp		260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device above these, or any other conditions beyond those "recommended" is not implied. Exposure to conditions above those "recommended" for extended periods of time may affect device reliability.

Required Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
Analog Supply	VDD_DNX2, VDD_XTAL, VDD_REF_SX, VDD_DNX1	1.5	1.6	1.65	V
Digital Supply	VDD_D, VREG_D_OUT	1.1	1.2	1.3	V
Battery Supply	VBATT_A3, VBATT_A4, VBATT_A5	3.0	3.3	3.6	V
Battery Supply	VBATT_A1, VBATT_A2, VBATT_D	1.7	1.8	2.0	V
AGC Control	VAGC	0		3.3	V
I/O Supply	VDD_IO	1.7	3.3	3.6	V
Operating Temperature	T	0	25	70	°C

Digital IO Specifications

Parameter	Symbol	Min	Typical	Max	Units
Output Logic Voltage SDA and SCL pins	VOH @ 3mA source	0.8 x VDD_IO			V
	VOL @ 3mA sink			0.2 x VDD_IO	V
Output Logic Voltage all other pins	VOH @ 2mA source	0.8 x VDD_IO			V
	VOL @ 2mA sink			0.2 x VDD_IO	V

Input Logic Voltage	VIH	0.7 x VDD_IO			V
	VIL			0.3 x VDD_IO	V

Integrated DVB-T Receiver Specifications

All specifications apply to using on-chip analog regulators with conditions defined in Operating Conditions.

Parameter	Condition	Min	Typical	Max	Units
Input Return Loss	75 Ω		6		dB
Supply (VBATT_A1, A2, A3, A4, A5) Ripple Susceptibility	(1KHz – 500KHz)			15	mVpp
RF Frequency Range		104		862	MHz
Channel Bandwidth			6, 7, 8		MHz

Tuner Specifications (IF Out)

All specifications apply to using on-chip analog regulators with conditions defined in Operating Conditions, measured at IF = 4.57 MHz and across RF frequency range.

Parameter		Symbol	Min	Typical	Max	Units
System						
Input Return Loss 75 Ω system		S_{11}		6		dB
RF Frequency Range		f_{RF}	44		885	MHz
Channel Bandwidth				6, 7, 8		MHz
Maximum Voltage Gain (Appendix 1)		G_{max}	87	94		dB
Gain Control Range		AGC	100	105		dB
Noise Figure		NF		5.5	7.0	dB
Output 1dB Compression			108	114		dBuVrms
3rd-order In-band Intermod Intercept (gain=50 dB)			-33.0	-26.0		dBm
IF LO Feedthrough Rejection	gain =0 – 70 dB	DCOS		-60	-45	dBc
I/Q Imbalance (gain = 50dB)		IQI		-60	-45	dBc
Supply (VBATT_A1, A2, A3, A4, A5) Ripple Susceptibility (1KHz – 500KHz)					15	mVpp
Loopthrough						
Gain	0dB Gain Mode	G_{LT}		0	3.5	dB
Noise Figure (LT Only)	0dB Gain Mode	NF_{LT}		7.5	10	dB
Channel Select Filter						
Channel Select Filter Band Edge Frequency Definition (measured at offset from center of band)	BW=6 MHz	FBE	NA	2.8	NA	MHz
	BW=7 MHz		NA	3.3	NA	MHz
	BW=8 MHz		NA	3.8	NA	MHz

Group Delay Across +/- Band Edge		BW=6 MHz	GD		300	400	ns
		BW=7 MHz			300	400	ns
		BW=8 MHz			300	400	ns
In-Band Amplitude variation		BW=6 MHz			2	3	dB
		BW=7 MHz			2	3	dB
		BW=8 MHz			2	3	dB
Attenuation of adjacent analog channel (measured at offset from center of band)	BW= 6 MHz	Picture (4.25 MHz)		70			dB
		Sound (3.25MHz)		35	40		dB
	BW= 7 MHz	Picture (4.75 MHz)		70			dB
		Sound (3.75MHz)		34	40		dB
	BW= 8 MHz	Picture (5.25 MHz)		70			dB
		Sound (4.75MHz)		48	70		dB
Synthesizer							
Phase Noise	at 1 kHz Offset				-80	-75	dBc/Hz
	at 10 kHz Offset				-90	-85	dBc/Hz
	at 100 kHz Offset				-95	-90	dBc/Hz
Channel Switching Time					20	25	ms
Others							
IF Output Impedance (single-ended)					270		Ω
VAGC Input Impedance					40k		Ω

Current Consumption

The current consumption for analog and digital modes accounts for temperature and process variations. Typical condition applies to using on-chip regulators with typical conditions defined in Recommended Operation Conditions.

Parameter	Supply Pin		Min	Typical	Max	Units
Tuner-Demod Mode Loopthrough = OFF	VBATT_A1 + VBATT_A2	RF=50-300 MHz		116		mA
		RF=300-900 MHz		105		mA
	VBATT_A3 + VBATT_A4 + VBATT_A5			36		mA
	VBATT_D			140		mA
Tuner Mode IF = 4.57 MHz Loopthrough = OFF	VBATT_A1 + A2	RF=50-300 MHz		116		mA
		RF=300-900 MHz		105		mA
	VBATT_A3 + VBATT_A4 + VBATT_A5			52		mA
	VBATT_D			30		mA

Crystal Requirements

A fundamental mode crystal is required.

Parameter		Min	Typical	Max	Units
Xtal Frequency	Tuner only mode		24, 28.8 and 48		MHz
	Tuner-Demod mode		24, 27, 28.8 and 48		MHz
ESR			50	100	Ω
Frequency accuracy		-70		70	ppm

IF Frequencies Supported

Low IF (MHz)	Standard IF (MHz)	Bandwidth (MHz)	Comment
4.0, 4.57, 6.0, 7.2	36.15	6, 7, 8	Programmable channel BW

ESD Performance

All pins pass the ESD performance of 2000V using the Human Body Model (HBM), and of 200V using the Machine Model (MM).

Timing Specifications

MPEG-2 TS parallel output interface

The waveform for the MPEG-2 TS parallel output interface is shown in Figure 2. This interface has the following features:

- The maximum parallel output clock frequency is 36.57 MHz
- Selectable output clock frequencies.
- The output clock polarity can be inverted.
- The polarity of the MPEG valid and MPEG sync signals can be controlled.

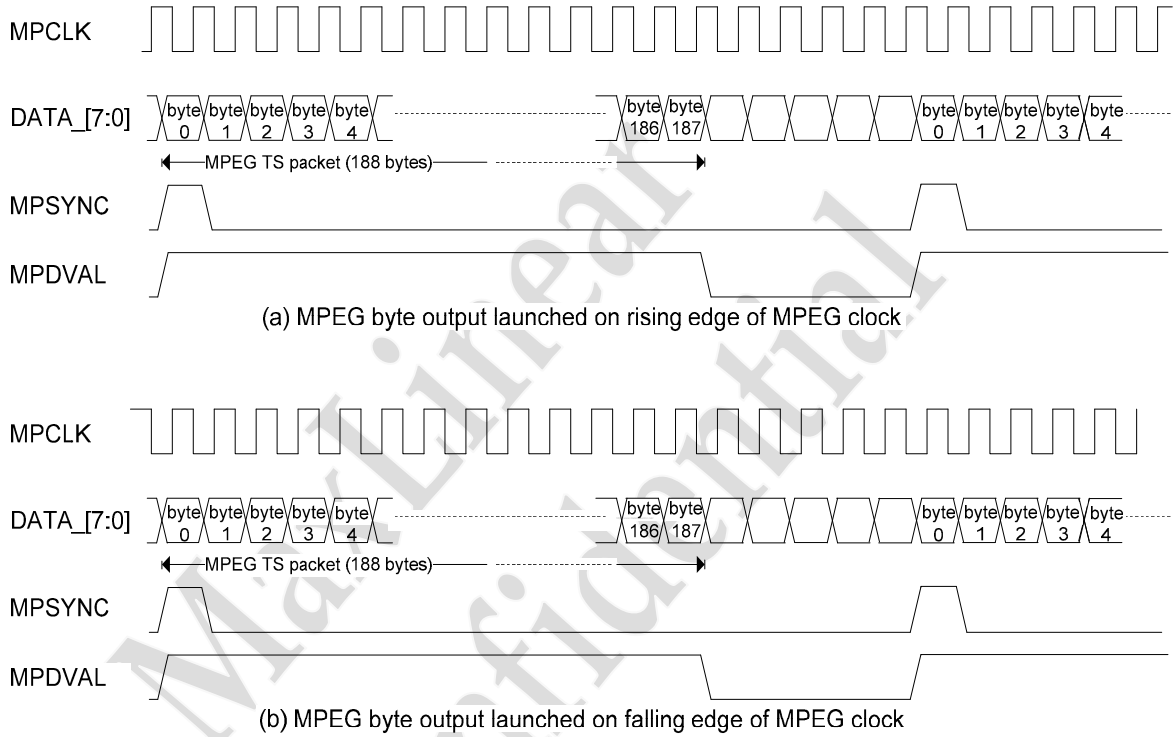


Figure 2: MPEG-2 TS parallel output interface waveform

MPEG-2 TS serial output interface

The waveform for the MPEG-2 TS serial output interface is shown in Figure 3. This interface has the following features:

- The maximum serial output clock frequency is 36.57 MHz
- Selectable output clock frequencies.
- The output clock polarity can be inverted.
- The endian-ness of the output data bits can be controlled.
- The polarity of the MPEG valid and MPEG sync signals can be controlled.
- 1-16 turn-around cycles can be inserted between two successive MPEG-2 TS frames.

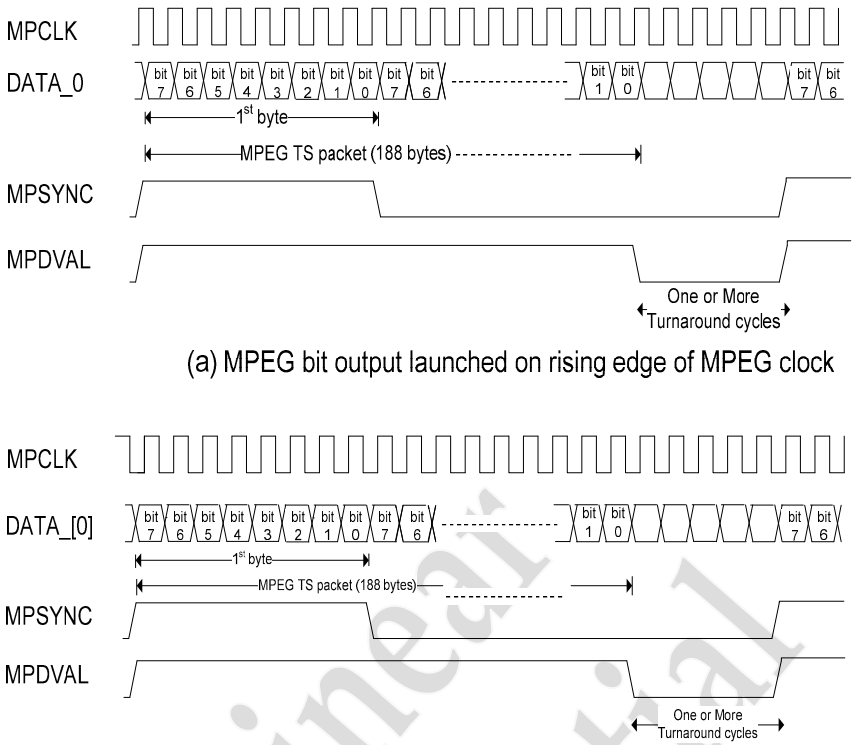


Figure 3: MPEG-2 TS serial output interface waveform

MPEG-2 TS output timing spec

Timing diagrams for the MPEG-2 TS output are shown in Figure 4, Figure 5 and Figure 6. The corresponding specifications are shown in Table 1.

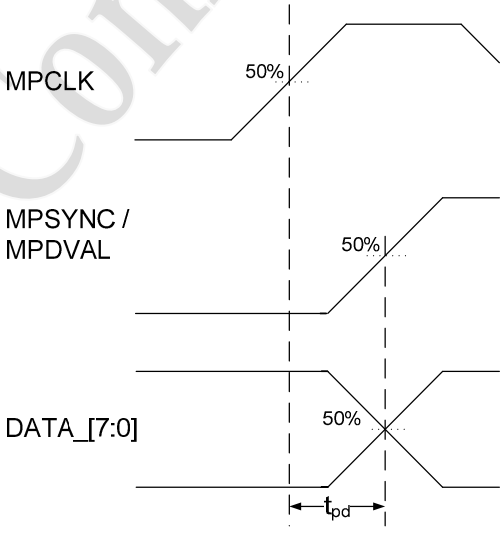


Figure 4: MPEG parallel output timing

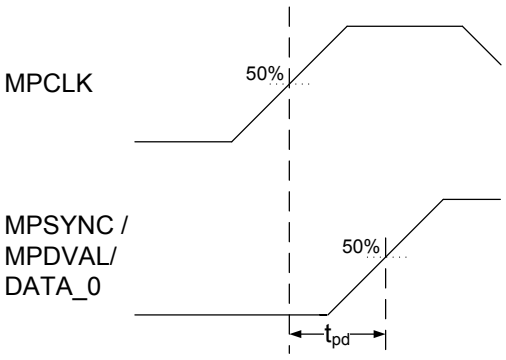


Figure 5: MPEG serial output timing

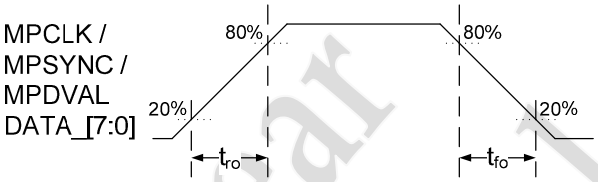


Figure 6: Output rise and fall time

Parameter	Symbol	Min	Typical	Max	Units
MPEG output					
MPEG clock output duty cycle		TBD	50	TBD	%
MPEG clock output frequency		2.285		36.57	MHz
MPEG output propagation delay (Figure 4 and Figure 5)	t_{pd}	TBD	2		ns
MPEG output rise time (Figure 6)	t_{ro}		TBD	TBD	ns
MPEG output fall time (Figure 6)	t_{fo}		TBD	TBD	ns

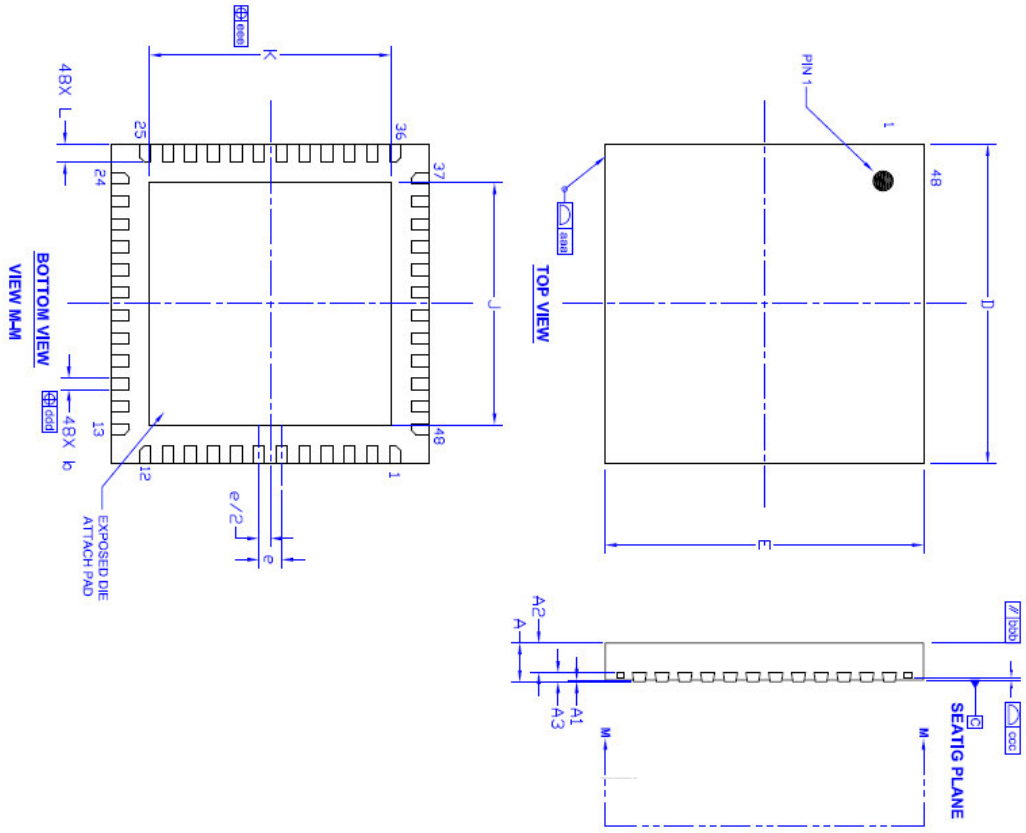
Table 1: Timing specifications

Ordering Information

Part Number	Package Type	Description
MxL101SF	QFN48	48-Pin QFN with no leads. Body size 7 x 7 x 0.85mm. Exposed backside paddle.

Packaging

QFN48 package dimensions: 7x7x0.85 mm³



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.8	0.85	0.9
STANDOFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	—	0.65	0.70
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.18	0.25	0.30
BODY SIZE	D		7 BSC	
	E		7 BSC	
LEAD PITCH	e		0.5 BSC	
EP SIZE	J	5.15	5.30	5.45
	K	5.15	5.30	5.45
LEAD LENGTH	L	0.30	0.40	0.50
PACKAGE EDGE TOLERANCE	aaa	—	—	0.15
MOLD FLATNESS	bbb	—	—	0.10
COPLANARITY	ccc	—	—	0.10
LEAD OFFSET	ddd	—	—	0.10
LEAD OFFSET	eee	—	—	0.10

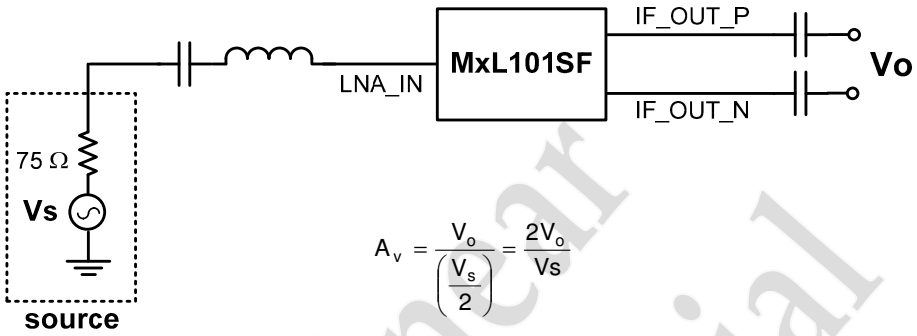
Application Circuit

Please contact MaxLinear Applications for more information.

Appendix

Voltage Gain Definition

This is defined as the voltage gain between the IF output and the voltage developed at the RF input assuming a 75 ohm matched input load.



$$A_v = \frac{V_o}{\left(\frac{V_s}{2}\right)} = \frac{2V_o}{Vs}$$

Revision History

Rev 1.0, Sept 14, 2008

1. First release

Rev 2.0, Feb 23, 2009

1. Change to proposed pinout with all corresponding changes
2. Split VOH for I2C and MPEG pins
3. Updated CSF specifications
4. Updated IF specifications
5. Updated SOC specifications
6. Added 3 frequencies for supported crystals
7. Changed supported IF to generic values
8. Added timing diagrams
9. Changed package info

Rev 2.1 June 4, 2009

1. VDD_D pin description: added "internally connected to V_REGD_OUT"
2. DATA_0-7 pin description: added "DATA_1-7 can be GPOs when not in use."
3. Pin description: added pin internal pull up and pull down information
4. Required Operating Conditions: changed VBATT_A5 from 1.8V to 3.3V
5. Updated available crystal frequencies
6. Updated the current consumption to match the estimates
7. Renamed pin 6 to VBATT_A5

Rev 2.2 August 4, 2009

1. Updated power consumption and current dissipation to match measurements.
2. Updated max NF spec